Amendments to the Specification:

Please replace the paragraph beginning at page 5, line 4, with the following redlined paragraph:

The circuit in Figure 2 illustrates an improved latch-type sense amplifier as provided by the present invention. The circuit comprises a modified latch consisting of PMOS transistors 110, 120, NMOS transistors 130, 140, and an additional set of NMOS transistors 170, 180. The bit line BL is connected through a PMOS transistor 150 and the bit line BLB is connected through a PMOS transistor 160. The NMOS transistor 200, controlled by the SAEN signal, is used for coupling the latch to a supply enabling the latch. A delayed version of the SAEN signal, *i.e.*, SAEND, is used to control switching off the PMOS pass transistors 150, 160. The signal SAEND is generated in the present implementation from a pair of inverters ~~180~~ 185, 190, though it may also be generated by various other means that can delay the signal as known in the art.